A STABLE GaAs 6-20 GHZ HIGH GAIN AND POWER TWA

Margaret M. Oda

Hewlett-Packard, Microwave Semiconductor Division
San Jose, California

Abstract

A stable power cascode distributed amplifier is demonstrated over the 6 to 20 GHz band. This monolithic GaAs traveling wave amplifier exhibits a minimum gain above 11 dB with +/- 0.5 dB of gain flatness over the band. The output power at the 1 dB gain compression point is over 24 dBm @ 20 GHz. The input/output return loss is better than 12 dB over the band. This chip was fabricated using a 0.4μm MESFET process and measures 3.02mm x 0.89mm (area of 2.7 mm^2). This power wideband amplifier employs 7 cascode stages. The excellent performance is achieved with the specially chosen transmission lines connecting the second gates and vias of each stage. This technique yields stability along with higher gain and power by eliminating the need for damping networks.

I Introduction

Many high gain cascode traveling wave amplifier (TWA) designs with many stages have employed damping networks to assure stability [1]. The typical series RC damping networks cause lower gain and power along with more negative gain and power slopes. By paying attention to how the gates of the common gate FETs (second gates) are connected together and to the backside via grounding schemes, damping networks can be avoided altogether and the full gain and power potential of the traveling wave amplifier can be realized.

This paper describes the design and performance of a high gain and power TWA which employs special stabilization techniques rather than the more conventional damping networks.

II TWA Design Choices

The first order design follows that of previous works on power TWA design [2] [3] [4] [5]. The design goal was to assure good power and gain performance from 6 GHz to 20 GHz. A cutoff frequency of 25 GHz was chosen to allow for process variations and extreme environmental conditions. Seven identical cascode stages were used with 390μm x 0.4μm FETs (see figure 5). Shunt capacitance on the drain of the common gate FET was used without any drain peaking transmission line. Series capacitors were used at the gates of the common source FETs (first gates) to improve power performance [2] [4] [5]. Thus, a coupling capacitor is not required at the input.

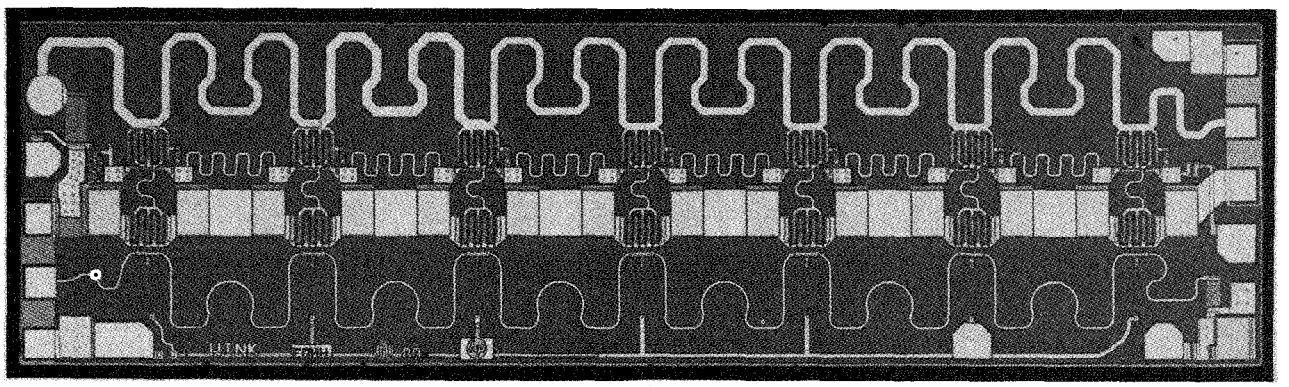

Figure 1: Photograph of chip.

CH2870-4/91/0000-0437$01.00 © 1991 IEEE

The shunt capacitance for the artificial gate transmission line is provided by the series combination of the coupling capacitor and the FET input capacitance as well as parasitics from the microstrip transmission line feeding the FETs. The shunt capacitance for the artificial drain transmission line is provided by the shunt MIM capacitor and the FET output capacitance as well as parasitics from the microstrip output transmission line. The gate and drain lines are terminated in 50Ω thin-film resistors in series with MIM bypassing capacitors which assure performance down to 6 GHz.

The second gates are biased with schottky diodes so that drain voltage variations will not significantly affect the second gate bias [6]. The nominal power bias point was chosen to be 9V, 360mA. With only drain bias applied, the amplifier operates at I_{DSS} with the second gates biased at 2.1V and the first gates self-biased to ground through a resistor. The chip size is 3020μm x 890μm (see figure 1 for die photo).

III Stabilization Technique

In any good amplifier design, one must address the issue of stability. Any two port network is unconditionally stable if the real part of the input and output impedances remain positive for all passive load and source impedances, respectively. Negative resistance at the drain of the common gate FET results from inductance between the second gate and ground. In the early stages of this design, simulation experiments were conducted which analyzed the effect of this inductance on the overall TWA stability. In the simulations, the second gates were assumed to be isolated from each other at the frequencies of interest and the common source and common gate FETs of each stage were grounded with separate backside vias. The simulation results for the TWA gain and K factor in two cases are shown in figures 2 and 3. In both cases, a bypass capacitor of 2 pF was used on the second gate of each stage. In case one, 56 pH of via inductance was assumed. This resulted in a second gate series resonance at 15 GHz (approximately 65% of the FET f_T). In case two, 14 pH of via inductance was assumed which resulted in a series resonance at 30 GHz (approximately 130% of the FET f_T). Note that the TWA was unconditionally stable only in the second case. In the first case, the stability factor (K) dipped below 1 at 21.5 GHz. Thus, keeping the second gate series resonance high will help maintain the TWA's stability.

There are other feedback mechanisms which may lead to instability when grounding vias are shared between various components and FETs [6] [7]. One needs to decide exactly how grounding of the various FETs and components will be accomplished as well as how the second gates will be connected together for DC

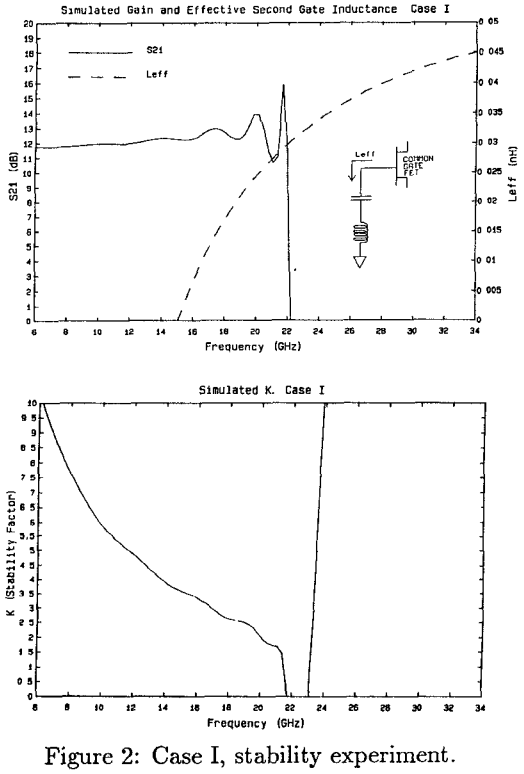

Figure 2: Case I, stability experiment.

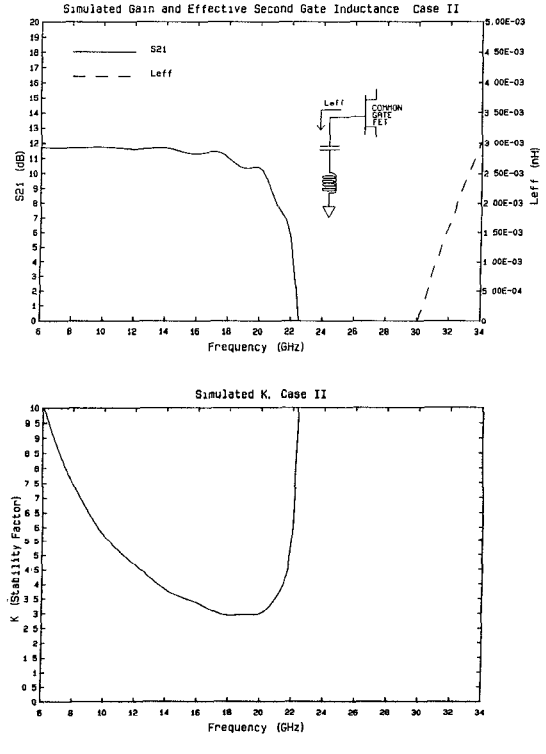

Figure 3: Case II, stability experiment.

biasing. These decisions are critical because they will affect the stability of the amplifier as well as the gain flatness. The grounding backside vias used have approximately 28 pH of inductance which is not negligible at 20 GHz. Due to chip area constraints and mechanical stability concerns, two grounding vias per stage are shared among the common source and common gate FETs as well as the shunt capacitance on the drain. In order to decrease the grounding via inductance, a low impedance transmission line was used between stages to connect adjacent vias. A high impedance transmission line was used to connect adjacent second gates so that they would be isolated from each other at microwave frequencies [7]. Figure 4 shows a photograph of a section of the chip and figure 5 shows the circuit schematic used to simulate the power TWA's performance. According to simulations, this final layout is stable without damping networks due to the use of the special techniques mentioned above. Thus, excellent gain and power performance can be achieved because damping networks are not needed to assure stability.

IV Measured Results

The design was fabricated using an f_T=23 GHz GaAs MESFET MMIC process [8]. Six wafers with this design have been evaluated on-wafer at a bias of 9 V and 360 mA. S parameters which were measured on-wafer from 6 to 20 GHz are shown in figures 6, 7 and 8 in log magnitude form. The gain is 11.9 +/− 0.5 dB, the input/output return loss is better than 12 dB, and the isolation is better than -25 dB.

All measured chips were proven to be unconditionally stable. This was proved by observing that the measured s-parameters satisfied the following conditions from 1.5 to 26.5 GHz [9]:

$$|S_{11}| < 1 \quad (1)$$

$$|S_{22}| < 1 \quad (2)$$

$$K > 1 \quad (3)$$

$$|\Delta| < 1 \quad (4)$$

Also, no spurious signals were observed from 26 to 40 GHz.

The output power at 1 dB gain compression and saturation was measured at 12GHz and 20GHz (See figure 9). P_{1dB} at 12 and 20 GHz was 27 and 24.8 dBm respectively. The corresponding values for P_{SAT} were 28.4 and 27.2 dBm.

Figure 10 shows both the measured gain and the simulated gain. Note that the measured gain is greater than 10 dB from 3 GHz to 26 GHz with gain flatness of +/- 1.4 dB. The input capacitance of the FETs on these measured wafers was significantly less than that of the FETs used in the simulations. This helps to explain why the measured data exhibits a larger bandwidth and lower gain than the simulation.

V Conclusion

It has been demonstrated that a stable cascode TWA design with high gain and power can be achieved without the use of damping networks. In addition to high gain and power, excellent gain flatness, return loss and isolation were also achieved in the 6 to 20 GHz band.

VI Acknowledgments

I would like to acknowledge Jerry Orr and Steve Cochran for their invaluable technical assistance with this design. I would also like to thank the HP MWTD

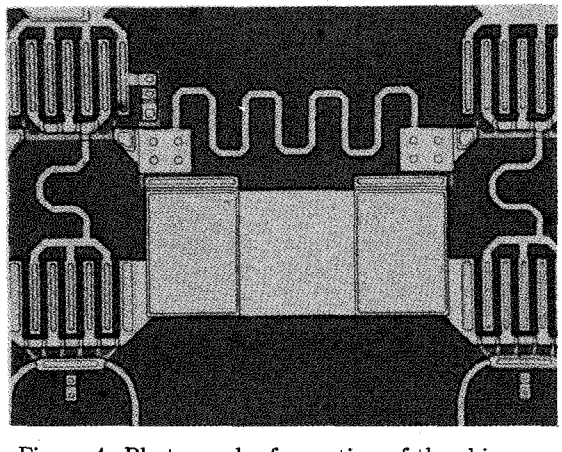

Figure 4: Photograph of a section of the chip.

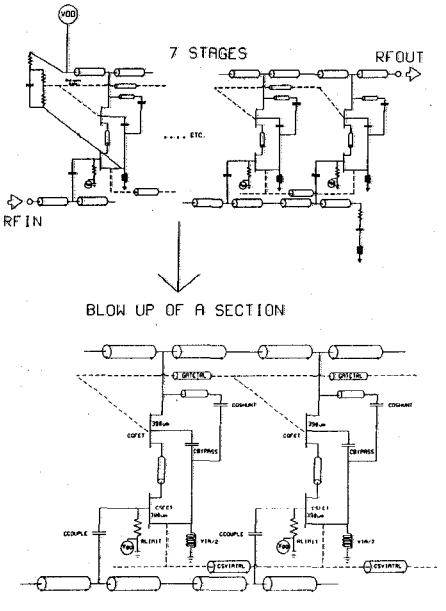

Figure 5: Circuit schematic of TWA.

GaAs IC group, the HP MSD group, the HP MWTD process group for wafer fabrication, M. Borg and D. Lee for their technical support and N. Nakamoto for help with the final manuscript.

References

[1] J. Orr, "A Stable 2-26.5 GHz Two-Stage Dual-Gate Distributed MMIC Amplifier," in *IEEE MTT-S Digest*, pp. 817–820, 1986.

[2] S. Prasad, J. B. Beyer, and I. Chang, "Power-Bandwidth Considerations in the Design of MESFET Distributed Amplifiers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 36, pp. 1117–1123, July 1988.

[3] J. Beyer, S. Prasad, R. Becker, J. Nordman, and G. Hohenwarter, "MESFET Distributed Amplifier Design Guidelines," *IEEE Transactions on Microwave Theory and Techniques*, vol. 32, pp. 268–275, March 1984.

[4] B. Kim and H. Tserng, "0.5W 2-21 GHz Monolithic GaAs Distributed Amplifier," *Electron. Lett.*, vol. 20, pp. 288–289, March 1984.

[5] Y. Ayasli, S. Miller, R. Mozzi, and L. Hanes, "Capacitively Coupled Traveling-Wave Power Amplifier," in *IEEE Microwave Millimeter-Wave Monolithic Circuits Symposium*, pp. 52–54, 1984.

[6] J. Orr. Private Communication.

[7] S. Cochran. Private Communication.

[8] D. D'Avanzo *et al.*, "A Manufacturable, 26 GHz GaAs MMIC Technology," in *Proceedings of the GaAs IC Symposium*, pp. 317–320, 1988.

[9] G. Gonzalez, *Microwave Transistor Amplifiers, Analysis and Design*. Prentice-Hall, Inc., 1984.

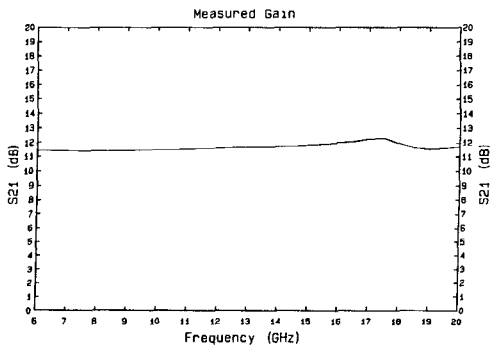

Figure 6: Measured S_{21} in dB.

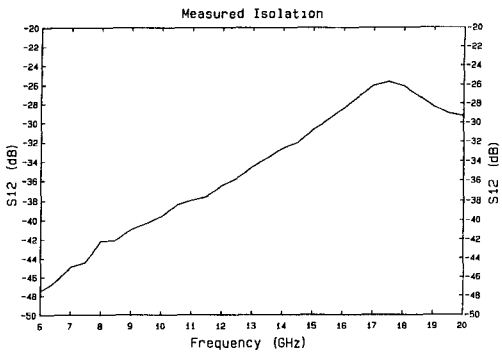

Figure 7: Measured S_{12} in dB.

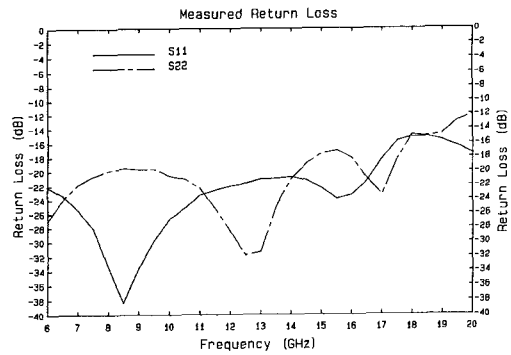

Figure 8: Measured S_{11} and S_{22} in dB.

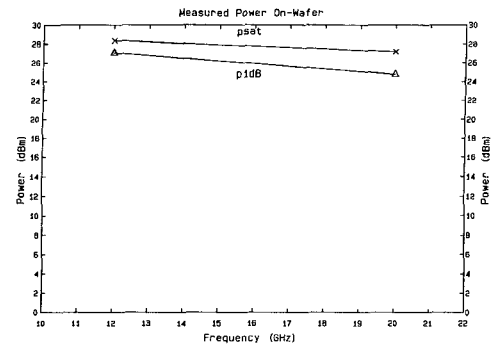

Figure 9: Measured power performance.

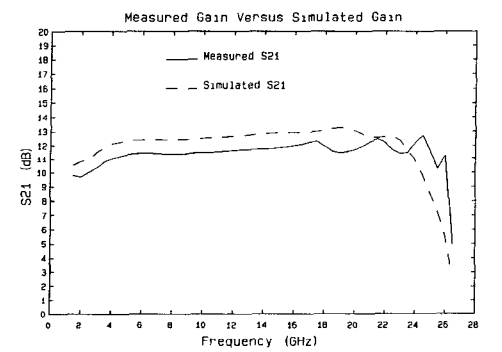

Figure 10: Gain: Measured vs Simulated.